Nano Energy (2015) 13, 433–441

Available online at www.sciencedirect.com

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High thermoelectric figure-of-merits from large-area porous silicon nanowire arrays

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Received 7 December 2014; received in revised form 20 February 2015; accepted 11 March 2015
Available online 20 March 2015

KEYWORDS
Thermoelectrics;
Silicon nanowire array;
Sandwich-structured composite;
Porosity;
Surface area

Abstract
High-density and large-area vertically aligned porous silicon nanowire arrays (SiNWAs) with different morphologies, such as various lengths, porosities and heterogeneous diameters, have been successfully fabricated on the two sides of silicon substrate using a simple metal-assisted chemical etching method. The porosity of the nanowires can be controlled by extending the etching time, and the surface area of the porous nanowires can reach as high as 547 $m^2 g^{-1}$. The thermoelectric properties of the SiNWA/Si/SiNWA sandwich structured composites (SSCs) were measured at room temperature and the figure-of-merit ZT for the corresponding porous SiNWAs were obtained. The results demonstrate that the ZT value of the SSC increases with the increasing porosity of SiNWA, and the porous SiNWAs with the highest surface area exhibit a high Seebeck coefficient up to 513 $\mu V K^{-1}$ and a thermal conductivity down to 1.68 $W m^{-1} K^{-1}$, resulting in a high ZT value of 0.493 at 300 K, which is 77 times higher than that of the bulk silicon (0.0064) and superior to all other reported results for SiNWAs system in terms of thermoelectric properties. The tremendously improved thermoelectric performance coupled with a scalable synthesis indicates the porous SiNWAs to be a greatly advanced candidate for the application in high-performance thermoelectric devices.

Introduction

Thermoelectric materials convert heat energy to electrical energy and are generally used for power generation and

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http://dx.doi.org/10.1016/j.nanoen.2015.03.011
2211-2855/

electronic refrigeration, which play an important role in solving the energy shortage and reducing environmental pollution from electrical power generation [1,2]. The thermoelectric efficiency is proportional to the merit value [3], which can be expressed as $ZT=S^2T/(\rho k)$, where T is the temperature, S is the Seebeck coefficient, ρ is the electrical resistivity, and k is the thermal conductivity. In order to obtain a maximum ZT value, S must be large enough to produce a large voltage under a small temperature difference, ρ must be small enough so as to minimize the Joule heat loss, and k must also be small in order to reduce the heat leakage and maintain the temperature difference. However, traditional thermoelectric materials experience difficult to meet these requirements simultaneously because they are interdependent as a function of the carrier concentration [4,5].

In last decades, with the rapid development of the nanofabrication technology, many researches [6-13] have demonstrated that semiconductor nanowires can overcome this contradiction and enhance their ZT values. In semiconductor nanowires, the thermal conductivity k can be greatly reduced due to severe phonon scattering on the interfaces and boundaries of the nanowires, meanwhile, the power factor S^2/ρ can be enhanced inherently by creating sharp features in electronic density of state [12], thus resulting in a much higher ZT value. Among various thermoelectric nanowires including Si [14-21], Ge [22], Bi [23], SiGe [24,25], InAs [26], BiTe [27,28] and PbTe [29,30] nanowires, Si nanowire (SiNW) is one of the mostly investigated TE structure due to its nontoxicity, comparatively easy synthesis, good stability under high temperature, abundant Si resource and ideal interface compatibility with Si-based electronic device. So far, there are many different types of SiNWs especially the individual one were investigated. Most of them are prepared by reactive ion etching method and generally have a smooth surface. In this case, good thermoelectric properties only appear for the SiNWs with small diameter and high doped concentration. Boukai et al. have reported a single smooth SiNW of about 20-nm-wide with a doped concentration of 7×10^{19} cm^{-3} showing $ZT\approx1$ at 200 K [20]. Nevertheless, Hochbaum group have reported that nanowires with rough surface fabricated by chemical electroless etching method can reduce thermal conductivity further due to the enhanced phonon-boundary scattering. They showed a SiNW with a rough surface, even at 50 nm in diameter, has a 100-fold reduction in thermal conductivity and the same power factor as bulk Si, and yields ZT=0.6 at 300 K [21]. However, for the real thermoelectric applications, only large-area SiNWAs would be more efficient and practical to be made as a useful device. Although theoretical calculations [31] showed that a higher ZT value can be obtained in laterally-coupled nanowire arrays than that of individual one due to the integrated effects of quantum confinement, electrons coupling and phonons boundary scattering, no experimental results proved such high ZT achieved. In fact, a much lower ZT value of SiNWAs are normally obtained, especially for the case of vertically aligned ones, this may be due to the arrays have low nanowire density or short length [32], large wire diameter [33] and polymer filler [34,35]. Also, recent research shows that bring nanopores into the nanomaterial can greatly decrease the thermal conductivity [36] and increase of the ZT value. For example, The theoretical and experimental results shows respectively that [37,38] the ZT value of ~0.4 were achieved for nanoporous Si film at room temperature (RT) which is 2 orders of magnitude over that of the bulk Si. Therefore, in this work, we have successfully synthesized large-area and high-density porous SiNWAs with various nanowire lengths and surface porosities, and systemically studied the thermoelectric properties of the bulk SSCs and SiNWAs at RT. It has found that porous SiNWAs possess a large surface area which could be useful in catalysis, super-capacitors and drug delivery, and the surface porosity is also found to have a significant effect on the ZT values of both SiNWAs and bulk SSCs, which are considered to be instrumentally important in designing future high-performance SiNWA based thermoelectric generators.

Experimental section

Porous SiNWAs were synthesized on 30×30 mm^2 single-crystal silicon wafers with a boron-doped concentration of 2×10^{19} cm^{-3} using the metal-assisted chemical etching method as described previously [39,40]. Si wafer pieces were cleaned subsequently in deionized water, acetone, ethanol and a boiling solution of H_2SO_4/H_2O_2 (4:1 v/v). The cleaned silicon pieces were then immersed in a solution of 0.01 M $AgNO_3$ and 4.8 M HF for 1 min to deposit Ag nanoparticles on both sides of the silicon pieces. Furthermore, the Ag nanoparticles deposited silicon pieces were immediately soaked in a solution of 0.2 M H_2O_2 and 4.8 M HF and etched at RT for different time, e.g. 60, 120, 180 and 240 min, respectively. Finally, the Ag residue on the SiNWAs was removed by washing in concentrated nitric acid and then dried under ambient atmosphere. The morphological and structural features of the SiNWAs and SSCs were investigated using field emission SEM (Hitachi S-4800) and high-resolution TEM (Jeol JEM-2010).

The porosity of the porous SiNWs was characterized by its surface area and mean pore diameter., The surface area was determined by the Brunauer–Emmett–Teller (BET) method using an Autosorb-IQ (Quantachrome) gas sorption analyzer. Approximately 20 mg of porous SiNWs was scratched from the wafers and degassed at 523 K overnight. The analysis was carried out under ultra-high purity grade of N_2 and He flow at 77.35 K in for a liquid nitrogen bath. The BET surface areas were calculated using a relative pressure between 0.05 and 0.30 prior to capillary condensation. The pore size distributions were determined f by the Barret–Joyner–Halenda (BJH) method.

For the Seebeck coefficient measurement, a layer of Al coated on the SiNWA with a thickness of 1 μm served as the electrode, which is deposited on both sides by magnetron sputtering. The polyimide film heater and the ceramic-made water cooler were used to form the temperature gradient between the center point on the top surface and the edge on bottom surface of the sample. Two thermocouples with an accuracy of 0.1 K were used to record the temperature during all experiments. The output thermoelectric potential (TEP) was measured by a source measure unit (Keithley 2612A). The photographs of the measurement setup are shown in Fig. A.1 (see Supporting information). The bulk SSC thermal diffusivity was measured by laser flash method (Netzsch LFA-457) as reported previously [40] and the bulk SSC electrical resistivity was examined by non-contact eddy current method (Napson EC-80P).

Results and discussion

Morphology characterization

By adjusting the etching time from 60 to 240 min, SiNWAs with different porosity and length are fabricated to examine the effect of the morphology on its thermoelectric properties. The scanning electron microscope (SEM) images in Fig. 1a are the morphologies of the SSC etched for 240 min. Typical samples have NW-bulk-NW sandwich structure, and the high-density vertically aligned SiNWAs are distributed uniformly over both the upper and lower surfaces of the bulk Si substrates. The diameter of the SiNWAs varies from 20 to 200 nm. The transmission electron microscopy (TEM) images from Fig. 1b-e display the individual porous SiNWs with the etching time of 60, 120, 180 and 240 min, respectively. Fig. 1f-i shows their corresponding high-resolution TEM images. The porosity of the SiNWs increase with the etching time, which is mainly resulted from the re-nucleation of the Ag nanoparticles on the sidewalls of the SiNWs.

More specifically, Ag nanoparticles are first deposited via Ag^+ reduction in $AgNO_3$/HF solution, and then induce the Si at the Ag/Si interface to be oxidized by H_2O_2 and then dissolved by HF, forming tunnels inward Si wafers as seen in Fig. 2. Due to the high density of Ag nanoparticles, neighboring tunnels might be merged together to form wider tunnels with the SiNWs in the between. During the etching process, the Ag^+ ions over the Ag^+/Si interface can diffuse upward to a lower Ag^+ concentration direction, and be reduced to Ag and form Ag clusters on the sidewalls of the silicon nanowires around the defective sites. For highly doped wafers, the dopants can incur many defective sites

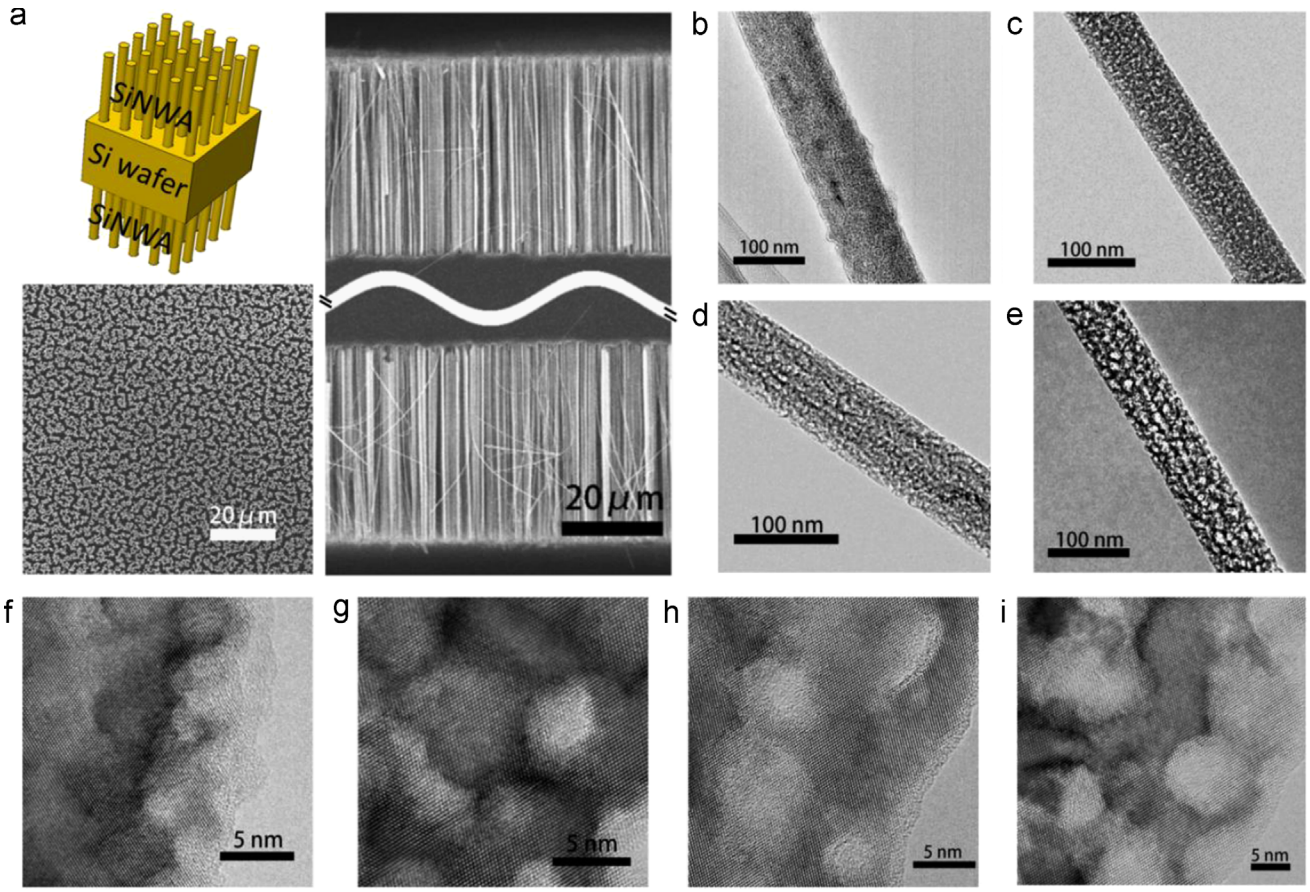

Fig. 1 Structural characterization of the SSC and porous SiNWs. (a) Cross-section and top-view SEM images of the SSC etched for 240 min. (b-e) TEM images and (f-i) their corresponding high-resolution TEM images of the individual porous SiNWs etched for different time. The etching time is 60, 120, 180, and 240 min for graph (b, f), (c, g), (d, h) and (e, i), respectively.

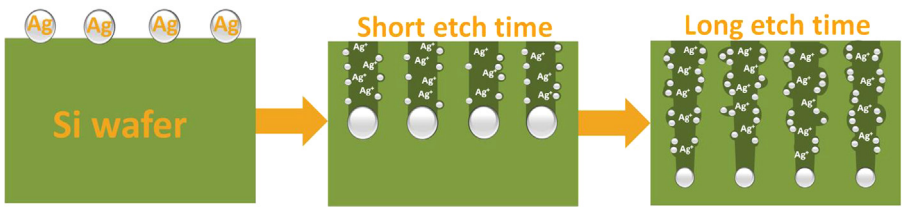

Fig. 2 Schematic illustration for the formation mechanism of porous SiNWs over highly doped silicon wafer formed by the metal-assisted chemical etching method.

on the nanowires, which serve as the nucleation centers for Ag clusters/nanoparticles and the etchable points for the formation of the following porous SiNWs. As the etching time increases, more Ag nanoparticles nucleate on the sidewalls of the SiNWs and lead to the increased porosity in SiNWA.

The nitrogen sorption isotherms of the porous SiNWs formed by various etching time are shown in Fig. 3a. The standard multipoint BET analysis shows the porous SiNWs with a high surface area increased with the etching time. For etching time of 60, 120, 180 and 240 min, the surface area of the porous SiNWs is 243, 367, 454 and 547 $m^2 g^{-1}$ respectively, which are far higher than that of smooth SiNWs (30 $m^2 g^{-1}$), and the value of 547 $m^2 g^{-1}$ are the highest one among the reported date for the porous SiNWs so far [41,42]. Fig. 3b shows the pore size distribution of the porous SiNWs calculated by the BJH method. The mean pore diameter of the porous SiNWs are 4.31, 7.79, 9.58 and 12.35 nm for the etching time of 60, 120, 180 and 240 min respectively, and which are consistent with the observation from high-resolution TEM analysis. The porous SiNWs with different pore diameter and large surface area have great potential in catalysis, biomedicine, energy harvesting and conversion. Table 1 summarizes the parameters of the SiNWs and the SSCs etched for different time, such as the surface area, the mean pore diameter and the fill factor of the SiNWs within the SiNWA, the length of the SSCs and the total length on two sides of the SiNWA. As the etching time is extended, the fill factor and growth rate of the SiNWs slightly decrease because the horizontal etching of the SiNWs is more dominant than that of the vertical one and leads to the increase of the number and size of the nanopores among the SiNWs.

Thermoelectric characterization

Fig. 4a exhibits the schematic measuring unit for the Seebeck coefficient of the SSC. By varying the heat voltage applied to the heater electrode, the TEP values of the SSCs with different etching time are acquired at various temperature differences $\Delta T = T_H - T_C$ (Fig. A.2, Supporting information), where T_H and T_C are the measured hot and cold spot temperature respectively. In Fig. 4b, the TEP value of SSCs increases gradually with the etching time under the same ΔT, which demonstrates that the porosity of the SiNWA can increase the Seebeck coefficient of the SSC. According to the definition $S = \mathrm{TEP}/\Delta T$, the Seebeck coefficient of the SSC is obtained as a function of the mean pore diameter (MPD) of the porous SiNWA at 300 K as shown in Fig. 4c. It reveals the Seebeck coefficients increased with the MPD of the corresponding porous SiNWA. When the MPD is zero, namely, a piece of nonporous silicon wafer, the Seebeck coefficient of the bulk silicon with a boron-doped concentration of 2×10^{19} cm^{-3} is 307 $\mu V K^{-1}$ at 300 K and similar to those previously reported values [38,43]. As the MPD increases from 4.31 to 12.35 nm, accordingly, the measured Seebeck coefficient increases from 323 to 376 $\mu V K^{-1}$ at RT. Fig. 4c also shows the thermal conductivity of the fabricated SSCs. When the MPD is 12.35 nm, the thermal conductivity of the SSC is 7.12 $W m^{-1}K^{-1}$ and much lower than that of bulk silicon (MPD=0 nm) at RT. In Fig. 4d, the electrical resistivity of the SSCs rises slightly from 5.4 to 6.8 mΩ cm with the increase of the porosity of the corresponding SiNWA from 0 to 12.35 nm. Combining the three thermoelectric parameters, the effects of the porosity of the SiNWAs on the ZT values of the SSCs are systematically examined. Fig. 4d shows that the ZT value of the bulk silicon is

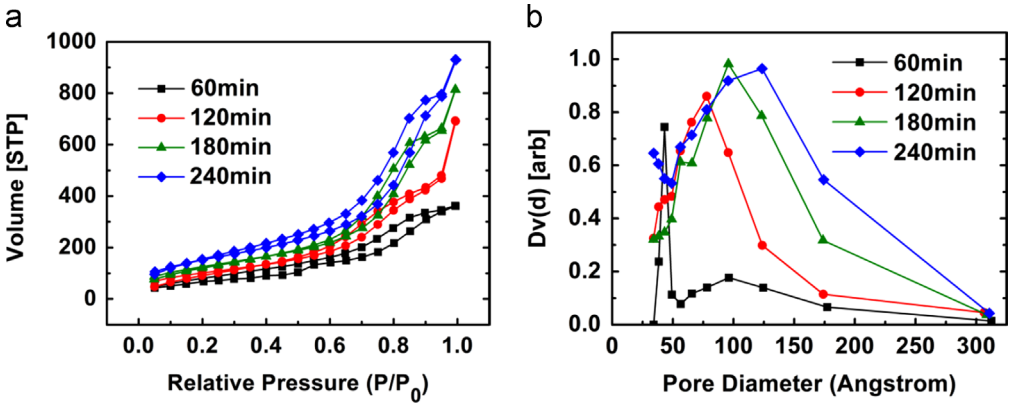

Fig. 3 Porosity characterizations of the porous SiNWs. (a) The nitrogen sorption isotherms and (b) their corresponding BJH pore size distributions obtained from the wafers with various etching time.

Table 1 The parameters for the SiNWs and SSCs formed by different etching time.

Etch time (min)	Surface areas of SiNW ($m^2 g^{-1}$)	Mean pore diameter of SiNW (nm)	Fill factor of SiNWs	Length (μm)	
				SSC	SiNWA
60	243	4.31	0.682	380	30.1
120	367	7.79	0.670	377	48.5
180	454	9.58	0.661	373	64.7
240	547	12.35	0.653	370	79.8

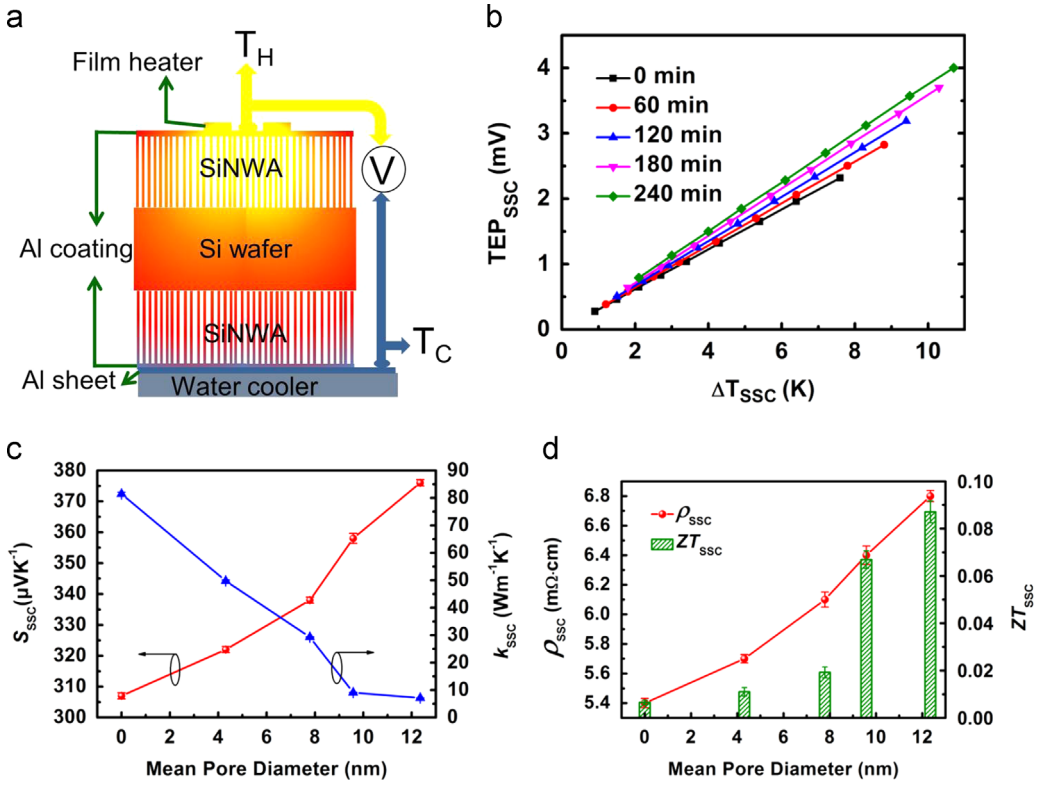

Fig. 4 Thermoelectric measuring results of the SSCs. (a) Schematic Seebeck coefficient measurement unit. (b) The thermoelectric potential (TEP) of the SSC etched for 0, 60, 120, 180 and 240 min at various temperature difference ΔT. (c)The Seebeck coefficient (S_{SSC}) and thermal conductivity (k_{SSC}) and (d) the electrical resistivity (ρ_{SSC}) and ZT value (ZT_{SSC}) of the SSC as a function of the MPD for the corresponding porous SiNWA at 300 K.

only 0.0064 at 300 K while that of the SSC with MPD of 12.35 nm can reach to 0.0871 at RT. This could be attributed to the following factors. One is the increase of the ZT value caused by porous SiNWA and the other one is the increase of the occupation ratio of porous SiWNA within a SSC.

For further investigation on the correlation between the thermoelectric properties of the SiNWAs and their surface morphologies, the Seebeck coefficient (S_{SiNWA}), the thermal conductivity (k_{SiNWA}) and the electrical resistivity (ρ_{SiNWA}) of the porous SiNWA with different porosity are conducted using a series of battery model (Eq. (1)), thermal resistance model (Eq. (2)) and electrical resistance model (Eq. (3)), respectively,

$$S_{SSC}\Delta T_{SSC} = S_{BSi}\Delta T_{BSi} + S_{SiNWA}\Delta T_{SiNWA} \quad (1)$$

$$\frac{L_{SSC}}{k_{SSC}} = \frac{L_{SiNWA}}{k_{SiNWA}} + \frac{L_{SSC} - L_{SiNWA}}{k_{BSi}} \quad (2)$$

$$\rho_{SSC}\frac{L_{SSC}^2}{(L_{SSC} - L_{SiNWA}) + L_{SiNWA}FF_{SiNWs}} = \rho_{BSi}(L_{SSC} - L_{SiNWA}) + \rho_{SiNWA}\frac{L_{SiNWA}}{FF_{SiNWs}} \quad (3)$$

where S_{BSi}, k_{BSi} and ρ_{BSi} represent the corresponding values of the bulk Si; L_{SSC} and L_{SiNWA} denote the length of the SSC and SiNWA; and FF_{SiNWs} is the fill factor of the SiNWs within the SiNWA as listed in Table 1. ΔT_{SSC}, ΔT_{SiNWA} and ΔT_{BSi} represent the temperature decrease from the SSC, the SiNWA and the sandwiched Si layer in the SSC. Since the measured $\Delta T_{SSC} = \Delta T_{SiNWA} + \Delta T_{BSi}$, if the ratio of ΔT_{SiNWA}: ΔT_{BSi} in the SSC is known, the values of ΔT_{SiNWA} and ΔT_{BSi} can be obtained. Unfortunately, it is very difficult to calculate the ratio by any analytical and numerical methods in the case with combined two dimensional heat conduction and heat convection. However, the COMSOL simulation under the same conditions as those of the experiments can easily acquire the ratios of ΔT_{SiNWA}:ΔT_{BSi} for different samples. The detailed COMSOL simulation process is provided in Supporting information. Under the same heat voltage, the simulated ratios of ΔT_{SiNWA}:ΔT_{BSi} in the SSC sample etched for 60, 120, 180 and 240 min are 1:9.8, 1:5.0, 1:2.9 and 1:2.0, respectively. The results of the thermoelectric properties of the porous SiNWAs for different MPDs are shown in Fig. 5. As Fig. 5a demonstrates, the Seebeck coefficients of the porous SiNWAs increase with the increase of the porosity due to the energy filtering effect [44] and the phonon drag effect [18,20]. For the porous SiNWA with a mean pore diameter of 12.35 nm, the value of the S_{SiNWA} is enhanced by 67% compared with the bulk silicon wafer at 300 K, which is lower than the reported Seebeck coefficient enhancement, where a ~3 times enhancement in the SiNWA is claimed compared to the bulk silicon at RT [45]. In addition, the electrical resistivity of the porous SiNWA in Fig. 5a increases with an increased porosity due to strong electron scattering. The electrical resistivity of the porous SiNWA covered by the nanopores with a mean diameter of 12.35 nm is 9.5 mΩ cm, which is 76% higher than that of the bulk silicon wafer at RT and contrary to those reported by Fischer et al. [46] and Hu et al. [47], where the electrical resistivity of porous SiNW is

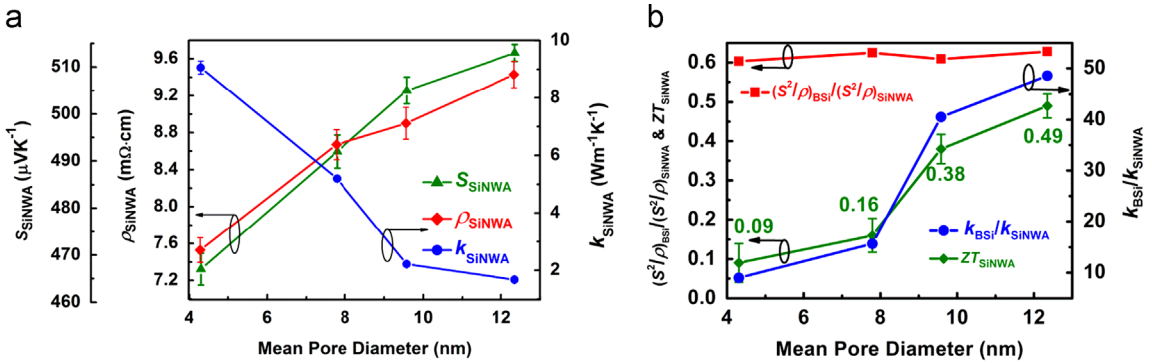

Fig. 5 The thermoelectric properties of porous SiNWAs for different mean pore diameter.(a) The Seebeck coefficients (S_{SiNWA}), the electrical resistivities (ρ_{SiNWA}), and the thermal conductivities (k_{SiNWA}) of the SiNWAs for various mean pore diameters at RT. (b) The effect of the MPD of the porous SiNWs on the ratio of the power factor of bulk Si compared with that of the SiNWA, i.e. $(S^2/\rho)_{BSi}/(S^2/\rho)_{SiNWA}$, and the ratio of the thermal conductivity (k_{BSi}/k_{SiNWA}) and the ZT value (ZT_{SiNWA}) of the SiNWA at 300 K. (See Supplementary information for the corresponding error analysis).

Table 2 Thermoelectric properties of SiNWAs at 300 K.

Method[a]	Diameter(nm)	Filler	$S(\mu V\ K^{-1})$	$\rho(\mu\Omega\ m)$	$k(W\ m^{-1}\ K^{-1})$	ZT	Reference
DRIE	~80	Polyimide	80	4.6	9.00	0.046	[34]
DRIE	80~90	SOG[b]	284	30	7.50	0.108	[32]
MACE	50~250	None	290	10	23.00	0.110	[33]
VLS	~200	Parylene	450	69	4.80	0.183	[35]
MACE	20~200	None	382	76	1.68	0.493	This work

[a]DRIE: Deep reactive ion etching; MACE: Metal-assisted chemical etching; VLS: vapor–liquid–solid growth.
[b]SOG: Spin-on-glass.

lower than that of bulk silicon or nonporous SiNW. However, the increase rate of the electrical resistivity becomes flat after the pore size reaches to 8 nm and above because the increase in the size rather than the number of the nanopores becomes the dominant factor for the resistivity increase, where the longer etching time will cause larger but fewer pores under identical conditions and the pores size will largely offset their number effect for electrical resistivity, therefore, the increase rate of the resistivity declines significantly. The thermal conductivity results show that porous SiNWAs have extremely low thermal conductivity and which is as low as 1.68 W $m^{-1}K^{-1}$at 300 K as seen in Fig. 5a due to the remarkable phonon scattering in boundaries and nanopores [40]. Moreover, the effect of the MPD of the porous SiNWA on the ratio of the power factor $(S^2/\rho)_{BSi}/(S^2/\rho)_{SiNWA}$, the ratio of the thermal conductivity k_{BSi}/k_{SiNWA}, and the ZT values of the porous SiNWAs have been examined as shown in Fig. 5b. The ratio of the power factor $(S^2/\rho)_{BSi}/(S^2/\rho)_{SiNWA}$ changes slightly with the MPD varying from 4 to 13 nm. However, the value of k_{BSi}/k_{SiNWA} increases dramatically from 8.9 to 48.5 as the MPD increases from 4.31 to 12.35 nm. More importantly, the ZT value of the SiNWA with an average nanopore size of 12.35 nm reaches 0.493 at 300 K, which is 77 times higher than that of the bulk silicon and close to that of the individual rough SiNW [21]. Therefore, compared with an individual rough SiNW, the porous SiNWAs with high-density and large-area should be more efficient and practical for thermoelectric devices. The recent results reported on thermoelectric parameters of SiNWAs have been summarized as comparison in Table 2. The SiNWAs synthesized by deep reactive ion etching and vapor–liquid–solid method normally have smooth surface and low array density, which need to be assisted by appropriate fillers for better performance. By contrast, the SiNWAs fabricated by metal-assisted chemical etching generally possess rougher pore wall and higher density which is crucial to improve their thermoelectric performance.

In order to better understand the impact of the occupation ratio of porous SiWNA on the thermoelectric properties of SSC, the SSC thermoelectric properties in the vertical direction at RT have been examined as a function of the ratio of the length of porous SiNWA to that of the non-etched silicon wafer in the SSC (L_{SiNWA}/L_{Si}) of different MPD. The detailed calculation process for the thermoelectric properties of the SSCs is given in the Supporting Information. As shown in Fig. 6, longer wires and larger porosity result in a higher Seebeck coefficient, a lower thermal conductivity and a slightly higher electrical resistivity, thereby leading a larger ZT value for the SSC. In terms of the thermal conductivity, the calculated plot for 9.58 nm pore is almost the same as that of 12.35 nm, which is considered to be contributed by the decrease of the number of the nanopores with lager diameter as discussed above. When the occupation ratio of porous SiNWA in the SSC reaches 50% at $L_{SiNWA}/L_{Si}=1$, thermoelectric characterization shows that the SSC with 12.35 nm pores has a Seebeck coefficient of 508 $\mu V\ K^{-1}$,

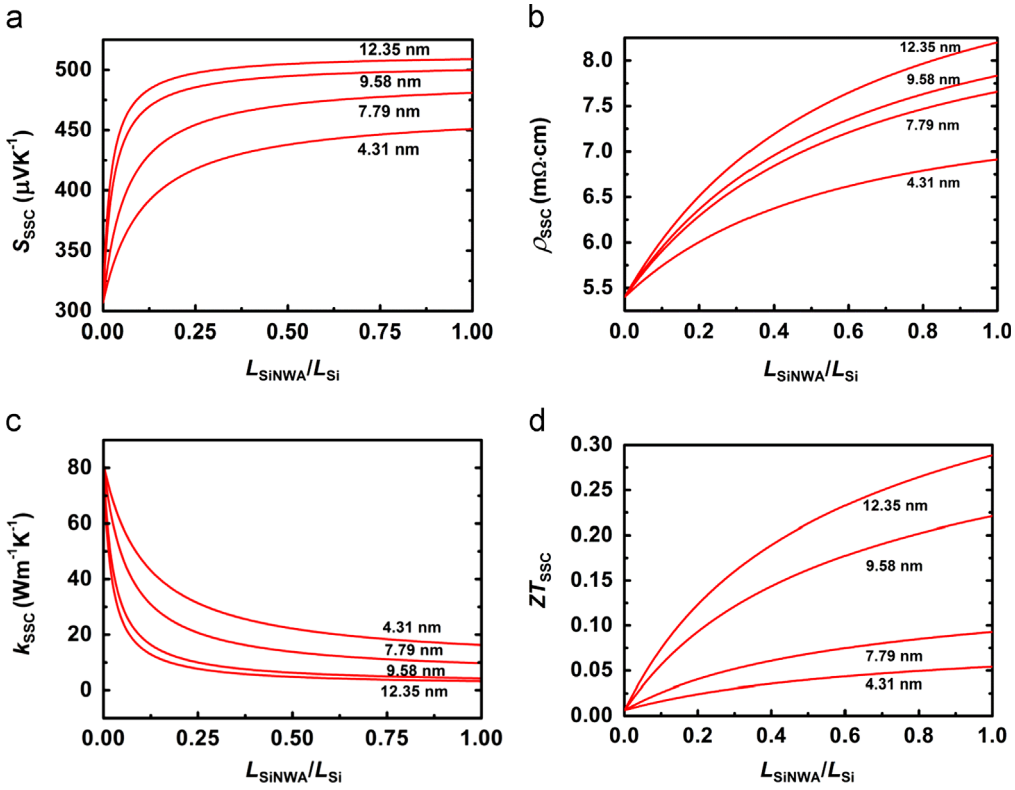

Fig. 6 Calculated thermoelectric properties of the SSCs as a function of the ratio of the length of its SiNWA with different MPD to that of the non-etched silicon wafer in the SSC (L_{SiNWA}/L_{Si}) at 300 K. (a) The Seebeck coefficient of the SSC (S_{SSC}), (b) the electrical resistivity (ρ_{SSC}), (c) the thermal conductivity (k_{SSC}) and (d) the thermoelectric figure of merit (ZT_{SSC}) of the SSCs. (See Supplementary information for error determination and calculate formulas).

thermal conductivity of 3.28 W mK^{-1}, electrical resistivity of 8.2 mΩ cm and a ZT value of 0.288 at 300 K. This ZT value is comparable to that of the nanostructured bulk SiGe alloy [48,49] and could be higher by adjusting the length and porosity of the corresponding SiNWA. Thus, the porous SiNWs incorporated bulk SSC could be an ideal candidate for high-performance thermoelectric devices.

Conclusion

Thermoelectric properties of the bulk SSCs and the high-density porous SiNWAs with different length and porosity have been systematically investigated, where the materials are controllably synthesized by metal-assisted chemical etching method. The ZT value of the SSC significantly increases with the increase of the length and porosity for the corresponding porous SiNWAs. Based on the widely-used battery, thermal and electrical resistance models, the ZT value of the porous SiNWAs with various surface porosities has been successfully obtained. In addition, the porous SiNWAs is able to increase the ZT value from 0.0064 for a piece of bulk silicon to 0.493 for a large porosity SiNWA at 300 K (surface area of 547 m^2 g^{-1} and mean pore diameter of 12.35 nm) due to the extremely low thermal conductivity caused by the strong phonon scattering and the significantly improved Seebeck coefficient incurred by the energy filtering, lateral coupling and phonon drag effect *etc*. Considering their tremendously improved thermoelectric performance, the bulk SSC and the high-density porous SiNWA fabricated in a controllable scale are very promising to be used for next generation thermoelectric devices.

Acknowledgments

This work was financially supported by the National Basic Research Program of China (No. 2010CB832905), the Program for New Century Excellent Talents in University (NCET-11-0043), the Fundamental Research Funds for the Central Universities and partially supported by the Key Scientific and Technological Project of the Ministry of Education of China (No. 108124).

Appendix A. Supporting information

Supplementary data associated with this article can be found in the online version at http://dx.doi.org/10.1016/j.nanoen.2015.03.011.

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